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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re Application of: | CHRISTOPHER A. BODE<br>JOYCE S. HEWETT | Group Art Unit: | 2123 |
| | | Examiner: | Eduardo Garcia Otero |
| Serial No.: | 09/815,446 | Conf. No.: | 7640 |
| Filed: | MARCH 22, 2001 | Atty. Dkt.: | 2000.068000/TT4149<br>CUSTOMER NO.: 23720 |

For: METHOD AND APPARATUS FOR PERFORMING FIELD-TO-FIELD COMPENSATION

# APPEAL BRIEF

| CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8 | |
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| DATE OF DEPOSIT: | May 5, 2006 |

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Signature

**MAIL STOP APPEAL BRIEF - PATENTS**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On April 3, 2006, Appellants filed a Notice of Appeal in response to a Final Office Action dated December 2, 2005, issued in connection with the above-identified application. In support of the appeal, Appellants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on April 7, 2006, the two-month date for filing this Appeal Brief is June 7, 2006. This Appeal Brief is being filed on or before the due date, therefore, it is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also

constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

**A fee in the amount of $500.00 for the filing fee of this Appeal Brief is due. The Commissioner is authorized to deduct said the(s) from Williams, Morgan & Amerson, P.C. PTO Deposit Account No. 50-0786/2000.068000/TT4149.** No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from Williams, Morgan & Amerson, P.C. PTO Deposit Account No. 50-0786/2000.068000/TT4149.

## I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

## II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

## III. STATUS OF CLAIMS

Claims 1-34 remain pending in this application.

The Examiner rejected claims 1-34 under 35 U.S.C. § 102(b) as being unpatentable over ***Ausschnitt*** (US 5,877,861).

## IV. STATUS OF AMENDMENTS

After the Final Rejection, no other amendments were made to any other claims.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed acquiring metrology data and performing a field-to-field based upon metrology data in order to determine a field-mean error. Embodiments of the present invention also relates to determining a wafer-mean error and comparing the field-mean error to the wafer-mean error. A residual-error analysis is performed, wherein the residual-error analysis includes determining whether significant residual error exists as a result of comparing the residual error with a pre-determined tolerance. The residual error analysis is based upon comparison of the wafer-mean error and the field-mean error. A field level adjustment and/or a wafer level adjustment is then performed based upon the residual error analysis. *See* Specification, page 7, lines 11-18.

In one aspect of the present invention, a method is provided for performing field-to-field compensation. At least one semiconductor device is processed. Metrology data is collected from the processed semiconductor device. A field-to-field metrology analysis is performed based upon the metrology data to determine a field-mean error. A wafer-mean error is determined. The field-mean error is compared to the to the wafer-mean error. Residual-error analysis is performed based upon the field-to-field analysis and the wafer-mean error. The residual-error analysis includes determining whether significant residual error exists as a result of comparing the residual error with a predetermined tolerance. The residual-error analysis is based upon the comparison of the wafer-mean error and the field-mean error data. A field-level adjustment

and/or a wafer-level adjustment is performed based upon the residual-error analysis. *See* Specification, page 4, line 22-page 5, line 2; page 12, line 1-page 14, line 9.

In another aspect of the present invention, an apparatus is provided for performing field-to-field compensation. The apparatus of the present invention comprises: a computer system (130); a manufacturing model (140) coupled with the computer system, the manufacturing model (140) being capable of generating and modifying at least one control input parameter signal; a machine interface coupled with the manufacturing model (140) and the computer system, the machine interface being capable of receiving process data from the manufacturing model (140) and the computer system; a processing tool (120) coupled with the machine interface, the processing tool (120) being capable of receiving at least one control input parameter signal from the machine interface and performing a manufacturing process; a metrology tool (150) coupled with the processing tool (120), the metrology tool (150) is capable of acquiring field-level metrology data; and a metrology data processing unit coupled with the metrology tool (150) and the processing tool (120). The metrology data processing unit is capable of organizing and analyzing the acquired field-level data and calculating at least one manufacturing error based upon a comparison of a field-mean error and a wafer-mean error for generating modification data. The manufacturing error includes a residual error determined as a result of comparing the field-mean error and the wafer-mean error. *See* Specification, page 5, lines 4-16; page 8, line 23-page 9, line 14; page 12, line 1-page 14, line 9.

In yet another aspect of the present invention, an apparatus is provided for performing field-to-field compensation. The apparatus of the present invention comprises: means for processing at least one semiconductor device; means for acquiring metrology data from the

processed semiconductor device; means for performing a field-to-field metrology analysis based upon the metrology data to determine a field-mean error; means for determining a wafer-mean error; means for comparing the field-mean error to the wafer-mean error; and means for performing residual-error analysis based upon the field-to-field analysis and the wafer-mean error. The means for performing the residual-error analysis includes means for determining whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance, the residual-error analysis being based upon the comparison of the wafer-mean error and the field-mean error data. The apparatus also comprises means for performing at least one of a field-level adjustment and a wafer-level adjustment based upon the residual-error analysis. *See* Specification, page 7, line 20-page 9, line 24; page 12, line 1-page 14, line 9.

In yet another aspect of the present invention, a computer readable program storage device that is encoded for performing field-to-field compensation. The method includes acquiring metrology data from the processed semiconductor device; performing a field-to-field metrology analysis based upon the metrology data to determine a field-mean error; determining a wafer-mean error; comparing the field-mean error to the wafer-mean error; and performing residual-error analysis based upon the field-to-field analysis and the wafer-mean error. The residual-error analysis includes determining whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. The residual-error analysis is based upon the comparison of the wafer-mean error and the field-mean error data. The method also includes performing at least one of a field-level adjustment and a wafer-level adjustment based upon the residual-error analysis. *See* Specification, page 7, line 20-page 9, line 24; page 12, line 1-page 14, line 9.

In another aspect of the present invention, a system is provided for performing field-to-field compensation. The system includes: a processing tool (120) to process at least one semiconductor device; a metrology tool (150) to acquire metrology data from the processed semiconductor device; and a controller to determine a field-mean error and a wafer-mean error based upon the metrology data and comparing the field-mean error and the wafer-mean error to determine a residual error. The controller is also adapted to determine whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. The residual-error analysis being based upon the comparison of the wafer-mean error and the field-mean error data. The controller is also adapted to perform at least one of a field-level adjustment and a wafer-level adjustment based upon the residual error. *See* Specification, page 7, line 20-page 9, line 24; page 12, line 1-page 14, line 9; page 14, line 11-page 16, line 17.

In another aspect of the present invention, an apparatus is provided for performing field-to-field compensation. The apparatus includes a controller to determine a field-mean error and a wafer-mean error based upon metrology data relating to a processed semiconductor device and comparing the field-mean error and the wafer-mean error to determine a residual error. The controller is also adapted to determine whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. The residual-error analysis is based upon the comparison of the wafer-mean error and the field-mean error data. The controller is also adapted to perform at least one of a field-level adjustment and a wafer-level adjustment based upon the residual error. *See* Specification, page 7, line 20-page 9, line 24; page 12, line 1-page 14, line 9; page 14, line 11-page 16, line 17.

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-34 are unpatentable under 35 U.S.C. § 102(b) over ***Ausschnitt*** (US 5,877,861).

## VII. ARGUMENT

The present invention is directed to performing a field-to-field metrology analysis based upon metrology data in order to determine a field-mean error. The invention is also related to determining a wafer-mean error and comparing the field-mean error to the wafer-mean error. The invention also relates to performing a residual-error analysis, which includes determining whether significant residual error exists as a result of comparing the residual error with a pre-determined tolerance. The residual error analysis is based upon comparison of the wafer-mean error and the field-mean error. A field level adjustment and/or a wafer level adjustment is then performed based upon the residual error analysis. The Examiner relies heavily on U.S. Patent No. 5,877,861 ***(Ausschnitt)***. ***Ausschnitt*** is merely directed to examining field overlay errors. ***Ausschnitt*** is directed to performing level to level metrology, which the Examiner mistakenly equates to the wafer-mean error metrology analysis called for by claims of the present invention.

Other misapplications of ***Ausschnitt*** by the Examiner include the misinterpretation of the terms "within level overlay errors" and "level to level field overlay errors" of ***Ausschnitt***. The Examiner misinterprets the term "within level overlay errors" by equating it to the field-level error. The Examiner also misinterprets the term "level to level field overlay errors" by equating it to the wafer-mean level analysis called for by claims of the present invention. ***Ausschnitt*** discloses a level-to-level description, which does not equate to the wafer-mean error, but merely

refers to overlay errors between one layer to another. The Examiner erred in equating the level-to-level metrology of ***Ausschnitt*** to the wafer-mean metrology, which refers to the average overlay error for a particular wafer as a whole, which as described in details below is not disclosed by ***Ausschnitt***.

Further, other elements of the claims of the present invention are also not disclosed by ***Ausschnitt***. For example, the element of comparing the field-mean error to the wafer-mean error, which the Examiner mistakenly equates to the suggestion in ***Ausschnitt*** that the correction factors are calculated from field turn error, alignment errors and level-to-level overlay measurements, is misapplied by the Examiner. This disclosure of ***Ausschnitt*** merely refers to the level-to-level errors and do not disclose or suggest wafer-mean errors. Further, ***Ausschnitt*** does not disclose comparing field-mean error to wafer-mean error. The mere assertion in ***Ausschnitt*** that correction factors are calculated from the field turn alignment errors and the level-to-level overlay measurements, does not equate to a disclosure of comparison between the field-mean error and the wafer-mean error. Therefore, all of the elements of the claims of the present invention are not taught, disclosed, or suggested by ***Ausschnitt.***

The specific claims of the present invention are discussed below.

**A. <u>Claims 1-34 Are Not anticipated Under 35 U.S.C. § 102(b) by U.S. Patent No. 5,877,861 (*Ausschnitt*).</u>**

The Examiner rejected claims 1-34 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,877,861 (***Ausschnitt***). Appellants respectfully traverse this rejection.

The Examiner's assertions in the Final Office Action dated December 2, 2005 are erroneous. ***Ausschnitt*** does not anticipate or make obvious all of the elements of claims of the present invention. In the Final Office Action dated December 2, 2005, the Examiner asserted that the level-to-level overlay errors of ***Ausschnitt*** equates to the wafer mean error. Further, the Examiner cites page 14 of the Specification of the present application, which discloses that the wafer mean error data relates to the average overlay error for a particular wafer as a whole from one process to another. It is clear that the specification discloses the wafer mean error data relating to average overlay error for a particular wafer as a whole. In contrast, ***Ausschnitt*** refers to particular layers of wafers, such as level A66 to the level B60 of Figure 8. ***Ausschnitt*** also refers to the fact that it is directed to the absolute error relating to level A and level B. ***Ausschnitt*** does not disclose an average overlay error for a wafer as a whole. Therefore, the Examiner's arguments in the Final Office Action dated December 2, 2005, do not disprove Appellants' arguments, which are discussed in further details below.

Further, in the Final Office Action dated December 2, 2005, the Examiner asserted that the Appellants' Specification and claims fail to disclose a definition of wafer mean error. Appellants respectfully assert that the claims do not need to define a wafer mean error since those skilled in the art having benefit of the present disclosure, upon reading of the claims, would readily decipher the context of the term "wafer mean error." As cited by the Examiner, the discussion regarding the term "wafer mean error data" in the Specification would allow those skilled in the art to readily decipher the meaning of the term "wafer mean error," which as describe herein, is clearly not anticipated by ***Ausschnitt***. Further, ***Ausschnitt*** does not make obvious various other elements of the claims of the present invention, such as comparing field mean error to a wafer mean error and performing a residual error analysis, which is not even

remotely contemplated by ***Ausschnitt***. These arguments are discussed in further detail below. Therefore, as described herein, various elements of the claims of the present invention are not taught, disclosed, or suggested by ***Ausschnitt***.

***Ausschnitt*** does not teach, disclose, or suggest all of the elements of claim 1 of the present invention. In the Final Office Action dated December 2, 2005, the Examiner misrepresents various terms disclosed in ***Ausschnitt*** to argue anticipation of various elements of claim 1. For example, the Examiner considers "level-to-level metrology" in ***Ausschnitt*** to be equivalent to wafer-mean error metrology analysis of the present invention. Other misapplications were also made in the Office Action, as described below. ***Ausschnitt*** merely discloses performing analysis of within-level overlay errors as well as of level-to-level field overlay errors. The level-to-level disclosure in ***Ausschnitt*** merely refers to multiple layers of the wafers, such as the "level A" 66 and the "level B" 60. *See* Figure 8, column 3, lines 44-49. ***Ausschnitt*** also refers to the fact that it is directed to the absolute error relating to level A and level B and not necessarily to the relative error between level A and level B. *See* column 3, lines 49-52. Appellants respectfully assert that the Examiner misunderstands the level-to-level error disclosed by ***Ausschnitt***. ***Ausschnitt*** is clear as to the fact that the level-to-level term relates to level-to-level field overlay error and not to the wafer-mean error called for by claims of the present invention. *See* column 4, lines 56-60. In other words, ***Ausschnitt*** is concerned with alignment of a field in level B to a field in level A and not to the wafer-mean error called for by claims of the present invention.

***Ausschnitt*** also refers to within-level field overlay errors. In other words, ***Ausschnitt*** is merely referring to checking for errors on one layer. This assertion is further bolstered by the

description in block 82 of Figure 12, which determines whether the analysis relates to a first level; if so, then the level A to level A overlay error is measured. *See*, Figure 12. If the analysis relates to an Nth level, then the level A to level B error is calculated. *Id.* Subsequently, the level to level error, which the Examiner mistakenly considers as being equivalent to wafer-mean error, is further described in block 86, which calls for calculating field terms after measuring the level A to level B overlay error. *See* Figure 12. Therefore, it is clear that the level-to-level description of ***Ausschnitt*** does not equate to wafer-mean error, but merely refers to overlay errors between one layer to another. Therefore, the Examiner erred in equating level-to-level metrology of ***Ausschnitt***, to the wafer mean error metrology called for by claim 1 of the present invention. Therefore, Appellants respectfully assert that the element of determining a wafer-mean error is not disclosed, taught, or suggested by ***Ausschnitt.***

Furthermore, the Examiner asserted that the comparison of the field-mean error to the wafer-mean error element called for by claim 1 of the present invention, is disclosed by the mere assertion in the summary of the invention relating to a description that correction factors are calculated from field-term error, alignment errors, and the level-to-level overlay measurement using the processor. Firstly, as Appellants described above, level-to-level error does not teach, disclose, or suggest wafer-mean error. Further, nowhere does ***Ausschnitt*** disclose comparing the field-mean error to the wafer-mean error. The mere assertion in ***Ausschnitt*** that the correction factors are calculated from the field-mean, field-term alignment errors and the level-to-level overlay measurements, does not equate to a comparison between the two. Therefore, the claim 1 element of comparing the field-mean error to the wafer-mean error is also not taught, disclosed, or suggested by ***Ausschnitt.***

Additionally, the Examiner attempts to read upon the element of performing residual error analysis based upon the field-to-field analysis and the wafer-mean error by citing col. 6, line 39, which refers to an equation using least squares best fit technique. The Examiner also points to col. 1, line 20, referring to a mere assertion relating to keeping an alignment error between levels below acceptable product tolerance. Appellants respectfully assert that these portions of the disclosure of ***Ausschnitt*** do not teach, disclose, or suggest the residual error analysis called for by claim 1 of the present invention. These calculations merely refer to errors relating to a level to level (i.e., layer to layer) field error, and does not disclose or suggest the residual error analysis based upon field-to-field analysis and the wafer-mean error, as called for by claim 1 of the present invention. Nowhere does ***Ausschnitt*** refer to performing a residual-error analysis based upon the field-to-field analysis as well as the wafer-mean analysis. Additionally, the residual-error analysis of claim 1 includes determining whether significant residual error exists as a result of comparing the residual error with a predetermined tolerance. ***Ausschnitt*** does not make such comparison. The mere assertion of the alignment error between levels being below product tolerance does not read upon this limitation. Furthermore, as described above, ***Ausschnitt*** does not disclose a residual-error analysis being based upon a comparison between wafer-mean error and a field-mean error. Firstly, as described above, ***Ausschnitt*** does not disclose determining a wafer-mean error. Secondly, ***Ausschnitt*** does not disclose or suggest determining comparing the wafer-mean error to the field-mean error. Therefore, several elements of claim 1 of the present invention are not taught, disclosed, or suggested by ***Ausschnitt.*** Therefore, the Examiner erred in maintaining the rejection of claim 1, and thus, claim 1 of the present invention is allowable.

Independent claim 11 calls for a system that includes a machine interface that is coupled to a manufacturing model and a computer system. The machine interface is capable of receiving process data from the manufacturing model and the computer system. The system also includes a metrology data processing unit that is capable of organizing and analyzing acquired field level data and calculating at least one manufacturing error based upon a comparison of a field mean error and a wafer mean error for generating medication data. As described above, ***Ausschnitt*** does not disclose a wafer mean error. Further, as described above, ***Ausschnitt*** does not disclose a comparison of a field mean error and a wafer mean error. Therefore, all of the elements of claim 11 are not taught, disclosed, or suggested by ***Ausschnitt***. Hence, the Examiner erred in maintaining the rejection of claim 11, and accordingly, claim 11 of the present invention is allowable.

Independent claim 15 of the present invention calls for means for performing a residual error analysis based upon a field-to-field analysis and a wafer-mean error. As described above, ***Ausschnitt*** does not disclose a wafer-mean error, nor does it disclose a comparison of a wafer-mean error and a field-mean error, as called for by claim 15 of the present invention. Further, as described above, ***Ausschnitt*** simply does not disclose a residual error analysis, which includes determining whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. Therefore, ***Ausschnitt*** simply does not disclose the residual error analysis of claim 15 of the present invention and, therefore, claim 15 is allowable. Hence, the Examiner erred in maintaining the rejection of claim 15, and accordingly, claim 15 of the present invention is allowable.

Independent claim 16 calls for a computer readable program storage device encoded with processing to perform various methods that include performing a residual error analysis. ***Ausschnitt*** does not disclose performing a residual-error analysis based upon the field-to-field analysis as well as the wafer-mean analysis. Additionally, the residual-error analysis of claim 16 includes determining whether significant residual error exists as a result of comparing the residual error with a predetermined tolerance. ***Ausschnitt*** does not make such comparison. The mere assertion of the alignment error between levels being below product tolerance does not read upon this limitation. Furthermore, as described above, ***Ausschnitt*** does not disclose a residual-error analysis being based upon a comparison between wafer-mean error and a field-mean error. ***Ausschnitt*** does not disclose determining a wafer-mean error. Further, ***Ausschnitt*** does not disclose or suggest determining comparing the wafer-mean error to the field-mean error. Therefore, ***Ausschnitt*** clearly does not disclose the residual error analysis of claim 16 of the present invention. Hence, the Examiner erred in maintaining the rejection of claim 16, and accordingly, claim 16 of the present invention is allowable.

Independent claim 26 calls for a system that includes a controller to determine a field mean error and a wafer mean error and perform a residual error analysis. The controller is also capable of determining whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. As described above, ***Ausschnitt*** does not disclose a wafer-mean error. Further, ***Ausschnitt*** does not disclose comparing a wafer-mean error and a field-mean error, as called for by claim 26 of the present invention. Also, ***Ausschnitt*** does not disclose a residual error analysis, which includes determining whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. Thus,

***Ausschnitt*** clearly does not disclose the residual error analysis of claim 29 of the present invention and therefore, claim 26 is allowable. Hence, the Examiner erred in maintaining the rejection of claim 26, and accordingly, claim 26 of the present invention is allowable.

Independent claim 29 calls for an apparatus that includes a controller that is capable of determining a field-mean error and a wafer-mean error based upon metrology data and comparing said field-mean error and said wafer-mean error to determine a residual error. The controller is also capable of determining whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. ***Ausschnitt*** does not disclose a wafer-mean error. Additionally, ***Ausschnitt*** does not disclose comparing a wafer-mean error and a field-mean error, as called for by claim 29 of the present invention. Also, ***Ausschnitt*** does not disclose a residual error analysis, which includes determining whether a significant residual error exists as a result of comparing the residual error with a predetermined tolerance. Thus, ***Ausschnitt*** clearly does not disclose the residual error analysis of claim 29 of the present invention and therefore, claim 29 is allowable. Hence, the Examiner erred in maintaining the rejection of claim 29, and accordingly, claim 29 of the present invention is allowable.

Independent claims 1, 11, 15, 16, 26, and 29 are allowable for at least the reasons cited above. Additionally, dependent claims 2-10, 12-14, 17-25, 27-28, and 30-34, which depend from independent claims 1, 11, 16, 26, and 29 respectively, are also allowable for at least the reasons cited above.

## VIII. CLAIMS APPENDIX

The claims currently under consideration, *i.e.,* claims 1-34, are listed in the Claims Appendix attached hereto.

## VII. EVIDENCE APPENDIX

There is no evidence relied upon in this Appeal with respect to this section.

## VIII. RELATED PROCEEDINGS APPENDIX

There are no related appeals and/or interferences that might affect the outcome of this proceeding.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims (claims 1-34) pending in the present application over the prior art of record. The undersigned attorney may be contacted at (713) 934-4069 with respect to any questions, comments, or suggestions relating to this appeal.

If for any reason the USPTO wishes to discuss this patent application, the USPTO is encouraged to contact the undersigned attorney at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON, P.C.
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## CLAIMS APPENDIX

1. (Previously Amended) A method, comprising:

processing at least one semiconductor device;

acquiring metrology data from said processed semiconductor device;

performing a field-to-field metrology analysis based upon said metrology data to determine a field-mean error;

determining a wafer-mean error;

comparing said field-mean error to said wafer-mean error;

performing residual-error analysis based upon said field-to-field analysis and said wafer-mean error, said residual-error analysis comprising determining whether significant residual error exists as a result of comparing said residual error with a predetermined tolerance, said residual-error analysis being based upon said comparison of said wafer-mean error and said field-mean error data; and

performing at least one of a field-level adjustment and a wafer-level adjustment based upon said residual-error analysis.

2. (Original) The method described in claim 1, further comprising processing said semiconductor device in a subsequent manufacturing process based upon said residual-error analysis.

3. (Original) The method described in claim 1, wherein processing at least one semiconductor device further comprises processing semiconductor wafers.

4. (Original) The method described in claim 1, wherein acquiring metrology data from said processed semiconductor device further comprises acquiring field-to-field metrology data analysis.

5. (Original) The method described in claim 1, wherein performing the field-to-field metrology analysis comprises:

acquiring overlay error data from at least one exposure field on each processed wafer;

calculating overlay errors for said exposure field based upon said overlay error; and

generating a set of field-mean error data.

6. (Original) The method described in claim 5, wherein calculating overlay errors for said exposure field comprises calculating at least one misregistration error.

7. (Original) The method described in claim 5, wherein calculating overlay errors for said exposure field comprises calculating at least one misalignment error.

8. (Original) The method described in claim 5, wherein performing residual-error analysis comprises:

generating wafer-mean error data;

comparing said wafer-mean error data to said field-mean error to calculate a difference between said wafer-mean error and said field-mean error data;

determining whether a significant residual error exists based upon said comparison of said wafer-mean error and said field-mean error data; and

using said wafer-mean error to perform manufacturing adjustments in response to a determination that significant residual error does not exist.

9. (Original) The method described in claim 8, further comprising:

calculating at least one field compensation parameter for at least one wafer-level adjustment in response to a determination that significant residual error exists; and

performing at least one wafer-level adjustment to compensate for at least one field-level error.

10. (Original) The method described in claim 8, further comprising:

calculating at least one field compensation parameter for at least one field-level adjustment in response to a determination that significant residual error exists; and

performing at least one field-level adjustment to compensate for at least one field-level error.

11. (Previously Amended) A system, comprising:

a computer system;

a manufacturing model coupled with said computer system, said manufacturing model being capable of generating and modifying at least one control input parameter signal;

a machine interface coupled with said manufacturing model and said computer system, said machine interface being capable of receiving process data from said manufacturing model and said computer system;

a processing tool coupled with said machine interface, said processing tool being capable of receiving at least one control input parameter signal from said machine interface and performing a manufacturing process;

a metrology tool coupled with said processing tool, said metrology tool being capable of acquiring field-level metrology data; and

a metrology data processing unit coupled with said metrology tool and said processing tool, said metrology data processing unit being capable of organizing and analyzing said acquired field-level data and calculating at least one manufacturing error based upon a comparison of a field-mean error and a wafer-mean error for generating modification data, wherein said manufacturing error comprises a residual error determined as a result of comparing said field-mean error and said wafer-mean error.

12. (Original) The system of claim 11, wherein said computer system is capable of generating field-level compensation modification data based on said manufacturing error for modifying at least one manufacturing parameter.

13. (Original) The system of claim 12, wherein said manufacturing model is capable of modifying said manufacturing parameter in response to said field-level compensation modification data.

14. (Original) The system of claim 13, wherein said processing tool is further capable of performing field-level manufacturing process.

15. (Previously Amended) An apparatus, comprising:

means for processing at least one semiconductor device;

means for acquiring metrology data from said processed semiconductor device;

means for performing a field-to-field metrology analysis based upon said metrology data to determine a field-mean error;

means for determining a wafer-mean error;

means for comparing said field-mean error to said wafer-mean error;

means for performing residual-error analysis based upon said field-to-field analysis and said wafer-mean error, said means for performing said residual-error analysis comprising means for determining whether a significant residual error exists as a result of comparing said residual error with a predetermined tolerance, said residual-error analysis being based upon said comparison of said wafer-mean error and said field-mean error data; and

means for performing at least one of a field-level adjustment and a wafer-level adjustment based upon said residual-error analysis.

16. (Previously Amended) A computer readable program storage device encoded with processing at least one semiconductor device;

acquiring metrology data from said processed semiconductor device;

performing a field-to-field metrology analysis based upon said metrology data to determine a field-mean error;

determining a wafer-mean error;

comparing said field-mean error to said wafer-mean error;

performing residual-error analysis based upon said field-to-field analysis and said wafer-mean error, said residual-error analysis comprising determining whether a significant residual error exists as a result of comparing said residual error with a predetermined tolerance, said residual-error analysis being based upon said comparison of said wafer-mean error and said field-mean error data; and

performing at least one of a field-level adjustment and a wafer-level adjustment based upon said residual-error analysis.

17. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 16, further comprising processing said semiconductor wafer in a subsequent manufacturing process based upon said residual-error analysis.

18. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 16, wherein processing at least one semiconductor device further comprises processing semiconductor wafers.

19. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 16, wherein acquiring metrology data from said processed semiconductor device further comprises acquiring field-to-field metrology data.

20. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 16, wherein performing the field-to-field metrology analysis comprises:

acquiring overlay error data from at least one exposure field on each processed wafer;

calculating overlay errors for said exposure field based upon said overlay error; and

generating a set of field-mean error data.

21. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 20, wherein calculating overlay errors for said exposure field comprises calculating at least one misregistration error.

22. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 20, wherein calculating overlay errors for said exposure field comprises calculating at least one misalignment error.

23. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 20, wherein performing residual-error analysis comprises:

generating wafer-mean error data;

comparing said wafer-mean error data to said field-mean error to calculate a difference between said wafer-mean error and said field-mean error data;

determining whether a significant residual error exists based upon said comparison of said wafer-mean error and said field-mean error data; and

using said wafer-mean error to perform manufacturing adjustments in response to a determination that significant residual error does not exist.

24. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, further comprising:

calculating at least one field compensation parameter for at least one wafer-level adjustment in response to a determination that significant residual error exists; and

performing at least one wafer-level adjustment to compensate for at least one field-level error.

25. (Original) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, further comprising:

calculating at least one field compensation parameter for at least one field-level adjustment in response to a determination that significant residual error exists; and

performing at least one field-level adjustment to compensate for at least one field-level error.

26. (Previously Amended) A system, comprising:

a processing tool to process at least one semiconductor device;

a metrology tool to acquire metrology data from said processed semiconductor device;

a controller to determine a field-mean error and a wafer-mean error based upon said metrology data and comparing said field-mean error and said wafer-mean error to determine a residual error, the controller also to determine whether a significant residual error exists as a result of comparing said residual error with a predetermined tolerance, said residual-error analysis being based upon said comparison of said wafer-mean error and said field-mean error data, the controller also being adapted to perform at least one of a field-level adjustment and a wafer-level adjustment based upon said residual error.

27. (Previously Presented) The system of claim 26, wherein said semiconductor device is a semiconductor wafer.

28. (Previously Presented) The system of claim 26, wherein said controller is adapted to control a processing operation upon a subsequent semiconductor device.

29. (Previously Amended) An apparatus, comprising:

a controller to determine a field-mean error and a wafer-mean error based upon metrology data relating to a processed semiconductor device and comparing said field-mean error and said wafer-mean error to determine a residual error, said controller also to determine whether a significant residual error exists as a result of comparing said residual error with a predetermined tolerance, said residual-error analysis being based upon said comparison of said wafer-mean error and said field-mean

error data, the controller also being adapted to perform at least one of a field-level adjustment and a wafer-level adjustment based upon said residual error.

30. (Previously Presented) The apparatus of claim 29, wherein said semiconductor device is a semiconductor wafer.

31. (Previously Presented) The apparatus of claim 29, wherein said controller is operatively coupled with a processing tool to control an operation of said processing tool.

32. (Previously Presented) The apparatus of claim 29, wherein said controller is capable of controlling a processing of a subsequent semiconductor device.

33. (Previously Amended) The method of claim 1, further comprising processing at least one additional semiconductor device.

34. (Previously Added) The method of claim 1, further comprising performing a field level adjustment and a field-to-field adjustment.